REMARKS

Claims 19, 21-28 and 30-70 are pending in the application. By this amendment, claims 19, 28, 38, 46, 54 and 63 are being amended to improve their form; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). New claims 71-76 are being added, to advance the prosecution of the application. No new matter is involved.

In paragraph 1 which begins on page 2 of the Office Action, claims 19, 21-28 and 30-70 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,717,224 of Zhang in view of U.S. Patent 5,309,264 of Lien et al. and U.S. Patent 5,880,797 of Yamada et al. In the Final Office Action of January 29, 2002, these claims were rejected as unpatentable over Zhang in view of Lien et al. Consequently, the rejection of the claims in the latest Office Action of July 8, 2002 is different to the extent that Yamada et al. is added to the combination of references. In this connection, Yamada et al. is said to show that the pixel electrode overlaps both the gate and drain lines so that, at the time of the present invention, one of ordinary skill in the art would have modified Zhang in order to have the pixel electrode overlap the gate and/or drain lines in order to increase the aperture by increasing the area of light transmission or in order to increase the capacitance. This rejection is respectfully traversed.

The Zhang and Lien et al. references are discussed on pages A13 and A14 of applicant's prior Preliminary Amendment of May 29, 2002. As further pointed out therein, the two references do not teach or suggest the limitations of the claims of the present invention, specifically the feature of overlapping the pixel electrode with the corresponding gate line extending in a row or column direction as set forth in the claims. Zhang does not teach that the pixel electrode (510 therein) overlaps the corresponding gate line (504 therein) in a row or column direction. Further, Zhang shows that the pixel electrode 510 specifically does not overlap the corresponding gate line in FIG. 5, as well as in FIG. 4A and 4B. Such reference also does not

discuss overlapping the pixel electrode with the corresponding drain line extending in either a row or column direction, because no row or column directions are discussed in Zhang.

As further pointed out in the Preliminary Amendment, Lien et al. does not remedy the deficiencies of Zhang, and specifically, does not teach or suggest the feature of overlapping the pixel electrode with the corresponding drain line extending in a row or column direction, as set forth in the claims. Further, Lien et al. teaches away from any such overlap, because Lien specifically states that the lines are adjacent to the electrodes and not overlapped with them, in Col. 4, lines 1-3 thereof. Therefore, Lien et al. teaches away from the claimed overlap, and cannot be combined with Zhang to show the claimed feature of overlapping the pixel electrode with the corresponding drain line extending in a row or column direction, as claimed herein.

Regarding U.S. Patent 5,880,797 of Yamada et al. which is combined with Zhang and Lien et al. in rejecting the claims under 35 U.S.C. § 103(a), such reference does not constitute prior art with respect to the claims of the present application. Yamada et al. was filed in the U.S. on December 24, 1996, which is less than one year before the May 7, 1997 filing date of the parent application for this divisional application. Applicant is enclosing a Declaration Under 37 C.F.R. § 1.131 to show that the date of invention (in Japan) was on or before February 29, 1996, the filing date of Japanese patent application Hei 8-43675 by the inventor of the present U.S. application. Hei 8-43675 fully describes the features being claimed in the present application. Accordingly, Yamada et al. does not qualify as prior art with respect to the present invention, and should be removed as a reference.

In discussing the limitations of the claims, the Office Action of July 8, 2002 states at the bottom of page 3 thereof that the functional recitation "sufficient thickness to alleviate an influence on the liquid crystal layer from an electric field generated by the TFT, gate lines, and the drain lines" has not been given patentable

weight because it is narrative in form. In order to be given patentable weight, a functional recitation must be expressed as a "means" for performing the specified function. In view of this, independent claims 19, 28, 46 and 54, and dependent claims 38 and 63, are being amended to set forth such limitations in means-plus-function language, as suggested. For example, in the case of claim 19, the reference to the interlayer insulation film at the end of the claim is amended in order to recite "further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines." The other claims noted have been amended in similar fashion. Therefore, claims 19, 21-28 and 30-70 are submitted to clearly distinguish patentably in their amended form. Neither Zhang nor Lien et al. disclose an interlayer insulation layer having a function of alleviation influence on the liquid crystal layer from an electric field generated by the TFT, the gate lines, and the drain lines. The formation of a thick layer in order to alleviate the influences can only be attempted with an understanding that such influences of the electric field adversely affect the display quality, and that, therefore, the present invention cannot be viewed as obvious from references that do not recognize such problem.

The thickness of the interlayer insulation film disclosed in Zhang is 0.7 μm, and such reference neither discloses nor suggests a thickness anywhere close to 1.0 μm or greater in the manner of the present invention. For the sole purpose of insulating the layers, it is sufficient according to Zhang to provide an interlayer insulation film with a thickness of 0.7 μm. Without any recognition of the influences on the liquid crystal by an electric field, a person with ordinary skill in the art would avoid any increase in the thickness from a necessary thickness. Therefore, there would be no motivation for increasing the thickness of the interlayer insulation film to 1.0 μm or greater in the manner of the present invention.

New claims 71-76 are similar to prior claims 19, 28, 37, 46, 54 and 62, except that in each case the interlayer insulation film is defined as having "a thickness of at least 1 μm". Consequently, such claims are submitted to clearly distinguish patentably over the cited art.

In conclusion, claims 19, 21-28 and 30-70 and new claims 71-76 are submitted to clearly distinguish patentably over the art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Version with markings to show changes made:

IN THE CLAIMS:

Rewrite claim 19 as follows:

19. (Three Times Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding gate line extending in a row direction;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and <u>further comprising means for providing</u> the interlayer insulation film [has] <u>with</u> a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

Rewrite claim 28 as follows:

28. (Three Times Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a row direction;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, [wherein] and further comprising means for providing the interlayer insulation film [has] with a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

Rewrite claim 38 as follows:

38. (Twice Amended) The liquid crystal display as claimed in claim 37, [wherein] further comprising means for providing the interlayer insulation film [has] with a thickness sufficient to alleviate an influence on the liquid crystal layer

by an electric field generated by the thin film transistors, the gate lines, and the drain lines.

Rewrite claim 46 as follows:

46. (Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a column direction;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and <u>further comprising means for providing</u> the interlayer insulation film [has] <u>with</u> a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

Rewrite claim 54 as follows:

54. (Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a row direction;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, [wherein] <u>further comprising means for providing</u> the interlayer insulation film [has] <u>with</u> a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

Rewrite claim 63 as follows:

63. (Amended) The liquid crystal display as claimed in claim 62, [wherein] <u>further comprising means for providing</u> the interlayer insulation film [has] <u>with</u> a

thickness sufficient to alleviate an influence on the liquid crystal layer by an electric field generated by the thin film transistors, the gate lines, and the drain lines.